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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,015	11/05/2001	David M. Weber	01-379	6514

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LSI Logic Corporation
Corporate Legal Department
Intellectual Property Services Group
1551 McCarthy Boulevard, M/S D-106
Milpitas, CA 95035

EXAMINER

NGUYEN, VINH P

ART UNIT	PAPER NUMBER
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2829

DATE MAILED: 12/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/993,015

Applicant(s)

WEBER, DAVID M.

Examiner

VINH P NGUYEN

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 August 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 16-24 and 33-43 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 16-24 and 33-43 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

1. Claim 39 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 39, it is unclear what "a current mirror" and "a plurality of transistors" represent. Are they shown in any of drawings? It appears that the term "the at least one transistor" has not been recited previously, therefore this term is indefinite. the same as "circuit component"? Furthermore, it is unclear how the current mirror and the plurality of transistors are interrelated and associated with test circuitry in claim 18.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 16-24,33-34,38,40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakata et al (Pat # 5,355,081) in view of Dukes et al (Pat # 5,570,035).

As to claims 16,18-20,33, Nakata et al disclose method for testing a plurality of integrated circuits (51) formed on a wafer as shown in figure 5. According to Nakata et al, as shown in figure 5, there is a network of signal paths (53,54) connect the integrated circuits to two or more connection points and each of the integrated circuits includes test circuitry (5,2,4,1) and each test circuitry (5,2,4,1) includes at least one visible component (light emitting diode "14") having an appearance. Nakata et al do not mention about the visible component would

permanently change its appearance in response to failing the test. However, Dukes et al teach that it would have been well known to use the fuse as an alternative indicator (see column 2, lines 33-37). It would have been obvious for one of ordinary skill in the art to provide a fuse as a visible indicator in the device of Nakata et al so that the visible indicator would change its appearance permanently.

As to claim 17, Nakata et al do not mention about the visible component including a fuse.

As to claims 20 and 40, Nakata et al teach that the signal paths (53,54) include a power supply signal path (54).

As to claims 21 and 41, it would have been well known that the signal paths (53,54) would include a clock signal.

As to claims 22 and 42, it would have been well known that the signal paths (53,54) would include a control signal.

As to claims 23 and 43, it appears that the signal paths are located on a scroll line (52).

As to claim 24, it appears that at least one of the signal paths is located on a die.

As to claim 34, it appears that when the fuse is used as “visible circuit component”, it would be destroyed.

As to claim 38, Nakata et al disclose the visible component (14) having at least one transistor as shown in figures 2 and 4.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 35-37 are rejected under 35 U.S.C 102(b) as being anticipated by Nakata et al (Pat # 5,355,081).

As to claims 35-36, Nakata et al disclose method for testing a plurality of integrated circuits (51) formed on a wafer as shown in figure 5. According to Nakata et al, as shown in figure 5, there is a network of signal paths (53,54) connect the integrated circuits to two or more connection points and each of the integrated circuits includes test circuitry (5,2,4,1) and each test circuitry (5,2,4,1) includes at least one visible component (light emitting diode "14") having an appearance.


As to claim 37, it appears that all the integrated circuits are cut off (see column 7, lines 28-34).

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2829

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is (703) 305-4914. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4900.


VINH P. NGUYEN
PRIMARY EXAMINER
ART UNIT 2858
11/21/03